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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	9

DATE MAILED: 12/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,381	LASSERRE, SERGE	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,11-13 and 17-20* is/are rejected.

7)☒ Claim(s) *3,4,6-10 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings were received on 25 August 2003. These drawings are approved by the Examiner.

Specification

2. Applicant is requested to update any data (continuation serial number, patent number, etc...) concerning co-pending or related applications listed in the specification.

The status of the parent applications on pages 1 and 11 should be updated as appropriate.

Claim Objections

3. Claims 12-17 are objected to because of the following informalities:

As per claim 12, line 2, "the address" should be --an address--.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 12 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Blumrich et al. (5,659,798).

As per claim 12, Blumrich et al. teaches, with reference to figure 3, a CPU 4 and a memory 8 ("local memory"), which is organized into a plurality of pages ("segments"). See column 7, lines 33-37. A memory management unit or MMU 5 in the CPU 4 maintains page tables which include a dirty bit for a page in each page table entry ("associating a plurality of indicator bits with the plurality of segments such that each segment has at least one corresponding indicator bit"). See column 16, lines 52-53. The page is marked as dirty if it has been written by an incoming DMA operation ("setting a first indicator bit associated with a first segment in the local memory to a first state in response to a DMA transfer"). The region of memory for the DMA transfer is selectable based on values placed in the appropriate registers in the DMA controller ("from a selectable location in a second memory to the first segment in the local memory"). See figure 3 and column 7, lines 2-6.

As per claim 17, as set forth above for claim 12, the "indicator bits" are dirty bits.

As per claim 18, Blumrich et al. teaches that dirty pages are written to a backing store.

As per claim 19, Blumrich et al. teaches that pages that are written to by an incoming DMA are marked as dirty (see column 16, lines 61-62). Blumrich et al. also teaches that the dirty bit is set if the version of a page has been changed since it was last written to a backing store (see column 16, lines 52-55). Therefore, Blumrich et al. teaches marking a page dirty if it is changed by the CPU 4.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 5, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baron et al. in view of Tanenbaum ("Modern Operating Systems").

As per claims 1 and 12, Baron et al. teaches an IC chip including a processor 4 and a memory ("local memory") 10, where the memory occupies at least a portion of the address space of the processor (i.e. the memory is not a cache memory exclusively). The memory includes 8 sectors ("plurality of segments") of 128 words each. See column 4, lines 45-53. Each word in each sector is associated with a valid bit ("plurality of indicator bits"). See column 5, lines 1-9. The IC chip can operate in a PRAM mode of operation (i.e. non-cache mode of operation). See column 4, lines 39-42. When operating in the PRAM (or STANDARD) mode of operation direct memory access (DMA) transfers occur between the program memory and the external memory using a DMA controller ("DMA circuitry"). See column 59-63. Even when operating in the PRAM mode, the valid bits are set by the DMA transfer ("operable to manipulate a selected portion of indicator bits...corresponding to the selectable portion of segments"). See column 8, lines 31-35.

Baron et al. does not teach the specifics of the DMA transfer, in particular that the controller transfers a selectable portion of segments from a selectable region of the external memory. Tanenbaum teaches DMA transfers where the CPU gives the DMA controller three

items of information for the DMA transfer: the disk (i.e. external) address of the desired data ("selectable region of a second memory"), the internal memory address where the desired data is to be placed, and the number of bytes to transfer ("selectable portion of segments"). See the first full paragraph on page 209 (lines 7-9). It would have been obvious to one of ordinary skill in the art to have implemented the standard DMA transfer operation, as taught by Tanenbaum, in the system of Baron et al., because Tanenbaum teaches that this procedure frees the CPU from low-level work, thereby allowing the CPU to more efficiently use its time. See page 209, lines 5-7.

As per claims 2 and 13, Baron et al. teaches that the plurality of bits are valid bits set by the DMA controller during a DMA transfer as detailed above for claims 1 and 12.

As per claim 5, Baron et al. teaches circuitry which checks the valid bit of the corresponding word in the sector (see column 5, lines 42-44). If the desired word is not valid, then a miss is indicated ("miss detection circuitry..."; see figure 2, "hit/miss" signal line connected through the gate logic to valid bits for each sector) and then data is retrieved from external memory using the provided address ("address circuitry..."). See column 5, lines 53-56.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (6,643,713) in view of Baron et al. in further view of Tanenbaum ("Modern Operating Systems").

Nakagawa et al. teaches a digital cellular telephone specification that includes (with reference to figure 2), a keyboard 235, a liquid crystal device 237 ("display"), RF modem 210, and an antenna 213. The CPU 227 and DSP chip 223 are connected to the LCD and keyboard over bus 229, the RF modem is indirectly connected to the DSP chip and the CPU, and the

antenna is indirectly connected to the RF modem. Nakagawa et al. further teaches a DSP/CPU integrated chip with a cache and DMA controller. See figure 7.

Nakagawa et al. does not teach that internal cache RAM of figure 7 includes a plurality of indicator bits, or that the DMA circuitry (see element 705 in figure 7) is operable to transfer a selectable portion of segments of the plurality of segments from a selectable region of a second memory and operable to manipulate a selected portion of indicator bits...corresponding to the selectable portion of segments.

Baron et al. teaches an IC chip including a processor 4 and a memory ("local memory") 10, where the memory occupies at least a portion of the address space of the processor (i.e. the memory is not a cache memory exclusively). The memory includes 8 sectors ("plurality of segments") of 128 words each. See column 4, lines 45-53. Each word in each sector is associated with a valid bit ("plurality of indicator bits"). See column 5, lines 1-9. The IC chip can operate in a PRAM mode of operation (i.e. non-cache mode of operation). See column 4, lines 39-42. When operating in the PRAM (or STANDARD) mode of operation direct memory access (DMA) transfers occur between the program memory and the external memory using a DMA controller ("DMA circuitry"). See column 59-63. Even when operating in the PRAM mode, the valid bits are set by the DMA transfer ("operable to manipulate a selected portion of indicator bits...corresponding to the selectable portion of segments"). See column 8, lines 31-35.

It would have been obvious to one of ordinary skill in the art to have modified Nakagawa et al. to replace the DSP/CPU integrated chip with the DSP chip of Baron et al. because Baron et

al. teaches at column 1, lines 38-39, that such a chip would provide an optimum use of silicon area.

The combination of Nakagawa et al. and Baron et al. does not teach the specifics of the DMA transfer, in particular that the controller transfers a selectable portion of segments from a selectable region of the external memory. Tanenbaum teaches DMA transfers where the CPU gives the DMA controller three items of information for the DMA transfer: the disk (i.e. external) address of the desired data ("selectable region of a second memory"), the internal memory address where the desired data is to be placed, and the number of bytes to transfer ("selectable portion of segments"). See the first full paragraph on page 209 (lines 7-9). It would have been obvious to one of ordinary skill in the art to have implemented the standard DMA transfer operation, as taught by Tanenbaum, because Tanenbaum teaches that this procedure frees the CPU from low-level work, thereby allowing the CPU to more efficiently use its time. See page 209, lines 5-7.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blumrich et al.

As per claim 20, Blumrich et al. does not teach a mode circuit which in one mode transfers only dirty segments and in another mode transfers the entire block. However it would have been obvious to one of ordinary skill in the art to have modified Blumrich et al. to incorporate a mode circuit such that in one mode transfers only dirty segments and in another mode transfers the entire block because this would increase the flexibility of the system. Blumrich et al. already teaches transferring to memory only dirty blocks. Incorporating the ability to transfer plural blocks without referring to the main memory would permit fast cache flushing on context changes.

Allowable Subject Matter

10. Claims 3-4, 6-10, and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 3 and 14, while Baron et al. teaches handling cache misses (i.e. when the processor requests access to data and the validity bit indicates the desired data is invalid), the cache miss procedure occurs in CACHE MODE and not the STANDARD MODE (which utilizes the DMA controller). Furthermore, the prior art of record does not teach or suggest, alone or in combination, stalling the processor in response to the miss signal until the DMA circuitry or DMA transfer sets a first valid bit corresponding to the first segment to a valid state, in combination with the other elements of the claims (i.e. claims 1-2-3 and 12-13-14).

With respect to claim 6, the combination of Baron et al. and Tanenbaum does not teach or suggest that the DMA circuitry is operable to transfer a block of data to a selected portion of segments in such a manner that a transfer to the first segment holding valid data within the selected portion of segments is inhibited, in combination with the other elements of the claims (i.e. 1-2-5-6).

With respect to claim 7 (and the claims depending therefrom), the prior art of record does not teach or suggest, alone or in combination, a processor having an address space connected to a local memory (which in not a cache memory as argued by Applicant at page 10 of the response filed 25 August 2003 in reference to the amended claims) occupying a portion of the address

space where the local memory responds to a transfer requests from the processor and has a data array arranged as a plurality of segments and a plurality of indicator bits, where each segment has a corresponding indicator bit, and DMA circuitry, connected to the local memory, which is operable to transfer data to a selectable portion of segments of the plurality of segments from a selectable region of a second memory and the DMA controller is operable to manipulate a selected portion of indicator bits corresponding to the selectable portion of segments, where the indicator bits are dirty bits indicating that a corresponding segment contains dirty data.

Blumrich et al. (5,659,798) teaches a page table containing dirty bits, where pages are marked dirty if written by incoming DMA, but the "indicator bits" of Blumrich et al. are located in the page tables in the MMU 5 and not in the memory 8 (see column 7, line 65 to column 8, line 5, and column 16, lines 61-67). The combination of claims 1 and 7 sets forth that the dirty bit indicators are located in the local memory. Furthermore, the kernel, and not the DMA, is operable to manipulate the bits. See column 17, lines 5-15. The combination of claims 1 and 7 sets forth that the DMA circuitry is operable to manipulate the dirty indicator bits.

Garnett (5,991,900) teaches a dirty RAM 124 in a bus bridge. However, the dirty bits of the dirty RAM are not part of the local memory data array as set forth in the present claims.

Response to Arguments

12. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendment to the claims.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
December 10, 2003